WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device provided with first electrodes formed on a semiconductor substrate and second protruded electrodes provided on said first electrodes, respectively, said method comprising the steps of:

a) forming a barrier metal on each one of said plurality of first electrodes, said step a) further comprising the sub-steps of:

- laminating a lowermost conductive metal layer on said first electrode, said lowermost conductive metal layer having a comparatively good joining property with said first electrode;

- laminating an intermediate conductive metal layer on said lowermost conductive metal layer; and

- laminating an uppermost conductive metal layer on said intermediate conductive metal layer, said uppermost conductive metal layer serving as a barrier layer for preventing said second protruded electrode from being diffused in said first electrode;

b) forming said second protruded electrodes on said barrier metals; and

c) implementing one or more predetermined test on said semiconductor substrate by applying signals to said semiconductor substrate,

wherein said step c) is carried out after said step a) and before said step b).

2. The method as claimed in claim 1, wherein,

in said step c), the signals are supplied to the semiconductor substrate by contacting said barrier metals with probes.

3. The method as claimed in claim 1, wherein said uppermost conductive metal layer is made of a material having resistance to reaction and adhesion with the metal used for the probe.

4. The method as claimed in claim 1, wherein said uppermost conductive metal layer is made of a material which can be easily alloyed with the material of the protruded electrode and has resistance to oxidation.

5. The method as claimed in claim 1, wherein said step b) is implemented only on those semiconductor chips which have been determined as good semiconductor chips during said step c).

6. The method as claimed in claim 1, said step b) further comprising the sub-steps of:

- forming a first metal coating, which will become said lowermost conductive metal layer, on substantially the entire surface on said semiconductor

substrate, said first metal coating having a layered structure of one or more layer having a comparatively good joining property with said first electrodes;

- forming a second metal coating, which will become a part of said intermediate conductive metal layer, on said first metal coating, said second metal coating having a layered structure of one or more layer having a comparatively good joining property with said first metal coating;

- forming third conductive metal layers, which will become a part of said intermediate conducive metal, by forming a resist provided with openings at positions corresponding to said first electrodes and having areas greater than the areas of the first electrodes, then forming third conductive metal layers in said openings such that the third conductive metal layers cover the second conductive coating, said third metal conductive layers having layered structure of one or more layer having a comparatively good joining property with said second metal coating and to said second protruded electrodes;

- forming fourth conductive metal layers, which will become said upper most conductive metal layer, on said third conductive metal layer, said fourth conductive metal layers having layered structure of one or more layer which easily alloys with the material of the second protruded electrodes and has resistance to oxidation;

- forming first conductive metal layers and second conductive metal layers by removing said first conductive metal coating and second conductive metal coating while using the third conductive metal layer and fourth conductive metal layer as masks.

7. The method as claimed in claim 6, wherein a weight of the fourth conductive metal layer is less than 2% (weight percentage) of the weight of the protruded electrode.

8. The method as claimed in claim 6, wherein said first conductive metal layer is made of a metal chosen from a group consisting of titanium (Ti), chromium (Cr), molybdenum (Mo) and tungsten (W), or of an alloy containing a metal chosen from a group consisting of titanium (Ti), chromium (Cr), molybdenum (Mo) and tungsten (W).

9. The method as claimed in claim 6, wherein said second conductive metal layer is made of a metal chosen from a group consisting of copper (Cu), nickel (Ni) and palladium (Pd), or of an alloy containing a metal chosen from a group consisting of copper (Cu), nickel (Ni) and palladium (Pd).

10. The method as claimed in claim 6, wherein said third conductive metal layer is made of a metal chosen from a group consisting of copper (Cu), nickel (Ni) and palladium (Pd), or of an alloy containing a metal chosen from a group consisting of copper (Cu), nickel (Ni) and palladium (Pd).

11. The method as claimed in claim 6, wherein said fourth conductive metal layer is made of a metal chosen from a group consisting of gold (Au), platinum (Pt), palladium (Pd), silver (Ag) and rhodium (Rh) or of an alloy containing a metal chosen from a group consisting of gold (Au), platinum (Pt), palladium (Pd), silver (Ag) and rhodium (Rh).

12. The method as claimed in claim 6, wherein said protruded electrode is made of a metal chosen from a group consisting of tin (Sn), lead (Pb), silver (Ag), indium (In) and bismuth (Bi) or of an alloy containing a metal chosen from a group consisting of tin (Sn), lead (Pb), silver (Ag), indium (In) and bismuth (Bi).

13. A semiconductor device having a semiconductor chip, first electrodes formed on said semiconductor chip, barrier metals formed on said first electrodes and having laminated structures, a plurality of second protruded electrodes, which serves as external connection terminals, formed on said barrier metals,

said barrier metal comprising:

a lowermost conductive metal layer laminated on said first electrodes and made of one or more conductive metal coating having a comparatively good joining property with said first electrodes;

an intermediate conductive metal layer laminated on said lowermost conductive metal layer and

made of one or more conductive metal layer having a comparatively good joining property with said lowermost conductive metal layer, at least one of said conductive metal layers serving as a barrier layer for preventing said protruded electrodes from diffused into said conductive metal layers; and

an uppermost conductive metal layer laminated on said intermediate conductive metal layers and made of one or more uppermost conductive metal layers made of a material which easily alloys with the material of said plurality of the uppermost conductive metal layers.

14. A method of manufacturing a semiconductor device comprising the steps of:

a) forming barrier metals on first electrodes provided on a chip of the semiconductor device;

b) implementing, after said step a), a predetermined test on the semiconductor device by applying a signal to the semiconductor device via at least one of the barrier metals; and

c) forming, after said step a),second protruded electrodes on the barrier metals.

15. The method as claimed in claim 14 wherein said step a) comprises a step of forming the barrier metals each having a multilayer structure having uppermost conductive metal layer which is made of a material which can be alloyed with a material of the second protruded electrodes and has a resistance to

reaction and adhesion with a material of probes used for said step b) and with a material of plated parts provided on the probes.

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